Abstracts

High efficiency submicron gate LDMOS power FET for low voltage wireless communications

G. Ma, W. Burger, Xiaowei Ren, J. Gibson and M. Shields. "High efficiency submicron gate LDMOS power FET for low voltage wireless communications." 1997 MTT-S International Microwave Symposium Digest 3. (1997 Vol. III [MWSYM]): 1303-1306.

A low cost, high efficiency silicon MOSFET using 0.6 /spl mu/m LDMOS (LV3) technology was developed in Motorola for high frequency (1-2 GHz) and low voltage (3.4-12.5 V) wireless applications. The LV3 devices can deliver 77% power added efficiency (PAE) with 12 dB gain, 28.7 dBm output power at 3.4 V and 850 MHz. The LV3 devices also can provide 70% PAE, 11 dB gain, 36 dBm Pout at 6 V, 850 MHz and 50% PAE, 9 dB gain, 33 dBm Pout at 5.8 V, 1.9 GHz. This is the best known RF performance for silicon devices at 3.4 V and 6 V.

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